**ECE 901 – Digital Systems Prototyping**

**Mini-Project 1**

**A Special Purpose Asynchronous Receiver/Transmitter (SPART)**



**Team:**

Kushagra Garg

Rohit Shukla

Vignesh Chandrasekaran

# Table of Contents

[Table of Contents 2](#_Toc379145684)

[Table of Figures 3](#_Toc379145685)

[1. Block Diagram 4](#_Toc379145686)

[2. Modules 5](#_Toc379145687)

[2.1 Baud Rate Generator 5](#_Toc379145688)

[2.2 Receiver 5](#_Toc379145689)

[2.3 Transmitter 6](#_Toc379145690)

[2.4 Driver 6](#_Toc379145691)

[3. Problems encountered 7](#_Toc379145692)

[4. Verilog Code 8](#_Toc379145693)

# Table of Figures

[Figure 1: Schematic of Top\_level module 3](#_Toc379145058)

[Figure 2: Schematic showing the interconnection between the Driver and SPART module 3](#_Toc379145059)

[Figure 3: Input synchronization in receiver module 4](#_Toc379145060)

# 1. Block Diagram

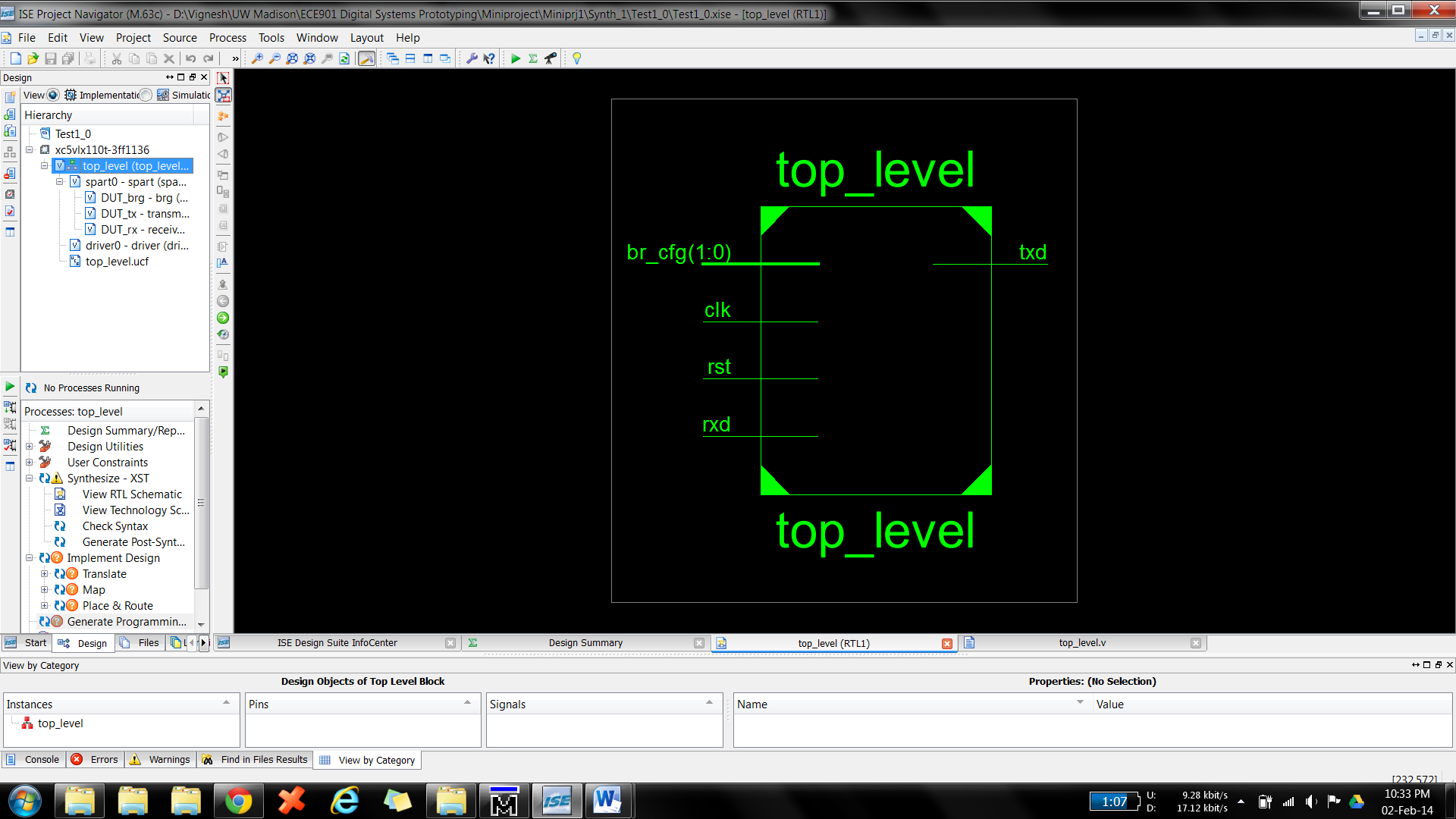


Figure 1: Schematic of Top\_level module

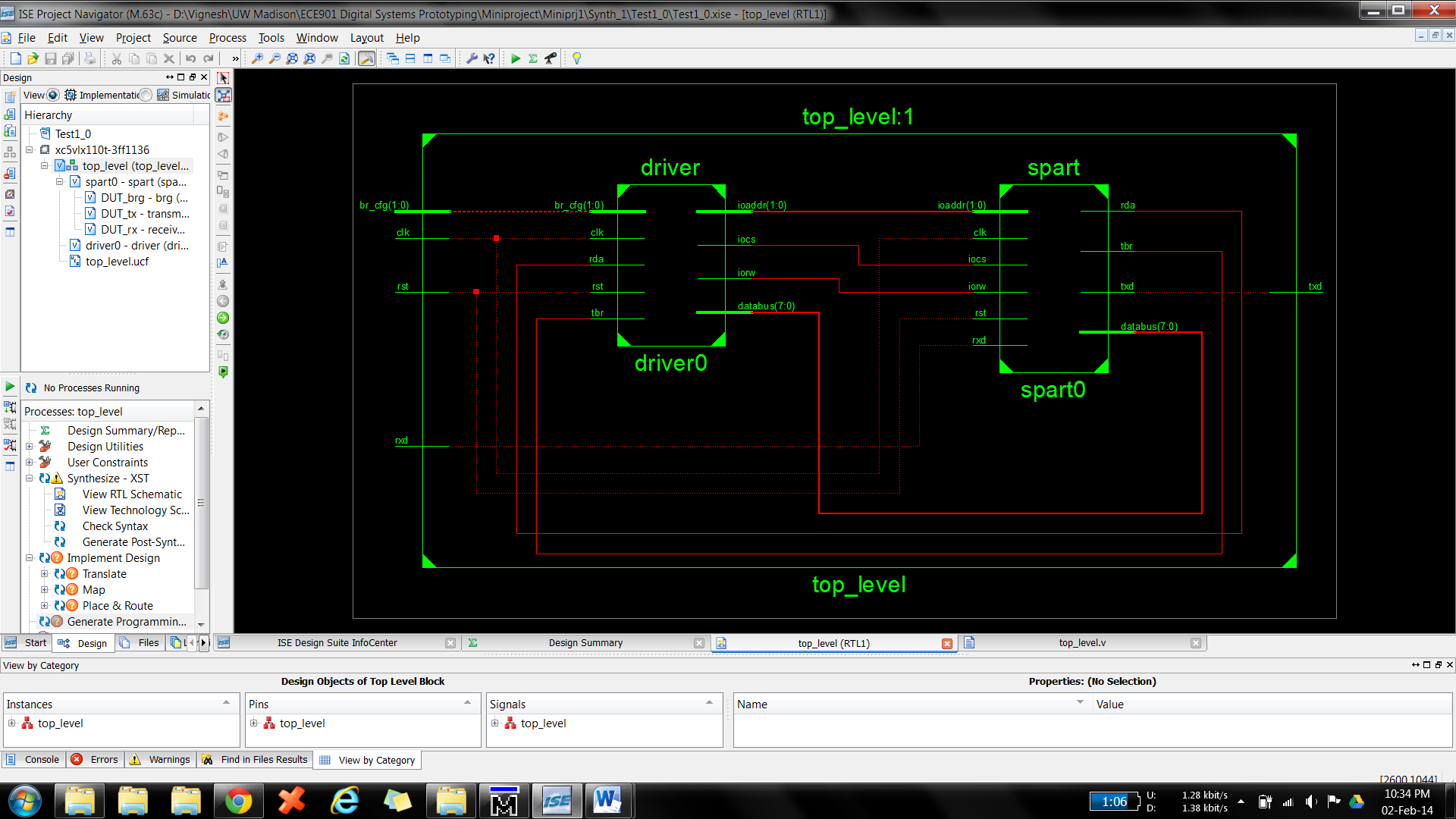


Figure 2: Schematic showing the interconnection between the Driver and SPART module

# 2. Modules

## 2.1 Baud Rate Generator

* BRG sets the division buffer to a default value of 650 upon reset which corresponds to the counter value for 9600 Baud rate at 100MHz clock rate.
* Depending on the value of IO Address which is set using the DIP switches, the division buffer gets loaded through the Databus with the appropriate data. Since the Div\_buffer is 2 bytes long, it’s loaded one byte at a time.
* BRG issues the enable signals for the transmitter and the receiver modules. The enable signal for the transmitter module is generated with the frequency that is 2n \* Baud rate, where n=4 in this case. The enable signal for the receiver module is generated when the counter that contains the corresponding value for the given baud rate runs down to zero. Therefore the frequency of the enable signal for the receiver signal is 16x the frequency of the enable signal for the transmitter.

## 2.2 Receiver

Receiver module in the spart architecture continuously receives asynchronous data from the computer at the baud rate set in computer’s HyperTerminal. Baud rate generator (BRG) outputs its signal brg\_en to the receiver module and whenever this signal is set, receiver module checks the one bit received input data. To circumvent the problem of meta-stability when receiving asynchronous data, we store the input bits in two one bit registers as shown in Fig. 1.

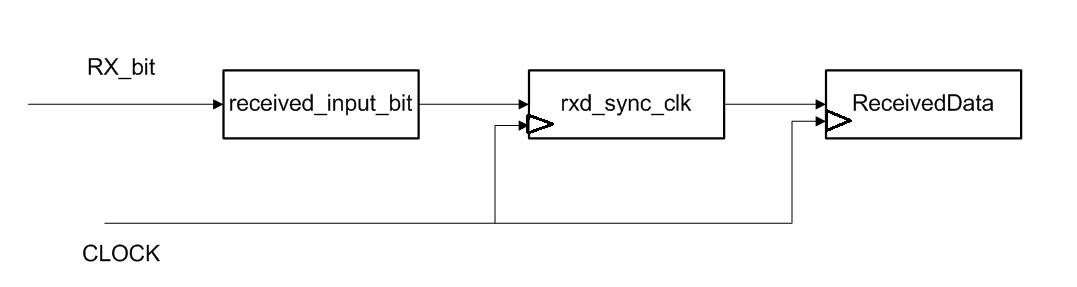


Figure : Input synchronization in receiver module

There is a four bit sample counter that counts the number of times brg\_en signal was asserted and a four bit sample accumulator counter that sums the received input bit. When the value of sample counter is 15, the receiver module checks the value MSB bit in sample accumulator counter. If the MSB value is 1, this indicates that receiver has received more number of bit ones than bit zeros. Thus receiver should interpret this as input bit 1. If the MSB value of sample accumulator is 0, the receiver will interpret that it has received bit 0. This implementation makes sure we sample the input data 16 times and do not read a wrong data that might occur due to spikes.

If the receiver sees bit zero for the first time, this indicates the start bit of input stream. A separate counter starts incrementing from 0 and goes on till 9, to ensure that all the 8 input bits have been received. Counter value is set to 1 when it reads the start bit. The received input bits that appear after the start bit are stored in a shift register named ReceivedData. After all of the 8 data bits have been stored, the value of counter is reset to zero and RDA signal is asserted to tell the processor that data is ready to be transferred from SPART. The RDA is reset when the top level SPART module sends a clr\_rda signal to the receiver module. The receiver will repeat the process of checking the start bit again.

## 2.3 Transmitter

## 2.4 Driver

# 3. Problems encountered

# 4. Verilog Code